REMARKS

Favorable reconsideration and allowance of the claims of the present application are respectfully requested.

In the present Office Action, Claims 4-6 stand rejected under 35 U.S.C. § 112, second paragraph as allegedly indefinite since the phrase "said bonded structure" in line 1 of each of the clams lacks sufficient antecedent basis in the base claim. In response thereto, applicants have deleted the term "bonded" from each of Claims 4, 5 and 6. The above amendment to Claims 4, 5 and 6 obviates the indefiniteness rejection. Reconsideration and withdrawal thereof are thus respectfully requested.

In addition to the above amendment to Claims 4-6, applicants have also amended Claim 1 to better define the sequence of processing steps claimed. In particular, Claim 1 has been amended to positively recite that during the forming of the undercutting shallow trench isolation regions, the back-gate is etched to a length which is less than a length of the overlying Si-containing layer, yet aligned to a lateral edge of said front polySi gate. Support for this amendment to Claim 1 is found at paragraphs [0061]-[0062] and in FIGS. 12 and 13 of the present application.

Applicants have also added new Claim 19 which is based on the subject matter of original Claims 1 and 12. Applicants note that the newly added claim is allowable over the art applied in the present Office Action given the Examiner's reason indicated at Page 9 of the Office Action.

Since the above amendment to Claim 1 and new Claim 19 do not introduce new matter into the instant application, entry thereof is respectfully requested.

Claims 1, 3, 5, 13-16 and 18 stand rejected under 35 U.S.C. § 102(b) as allegedly anticipated by U.S. Patent No. 5,273,921 to Neudeck, et al. ("Neudeck, et al."). Claim 2

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stands rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Neudeck, et al., U.S. Patent No. 6,342,717 to Komatsu, and Stanley Wolf and Richard N. Tauber Vol. I, "Silicon Processing for the VLSI Era". Claims 4 and 17 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Neudeck, et al. and Stanley Wolf, Vol II, "Silicon Processing for the VLSI ERA". Claims 6-12 stand rejected under 35 U.S.C. § 103 as allegedly unpatentable over the combined disclosures of Neudeck, et al. and Komatsu.

Concerning the § 102(b) rejection, it is axiomatic that anticipation under § 102 requires that the prior art reference disclose each and every element of the claim to which it is applied. In re King, 801 F.2d, 1324, 1326, 231 USPQ 136, 138 (Fed. Cir. 1996). Thus, there must be no differences between the subject matter of the claim and the disclosure of the prior art reference. Stated another way, the reference must contain within its four corners adequate direction to practice the invention as claimed. The corollary of the rule is equally applicable: Absence from the applied reference of any claimed element negates anticipation. Kloster Speedsteel AB v. Crucible Inc., 793 F.2d 1565, 1571, 230 USPQ 81, 84 (Fed. Cir. 1986).

Applicants respectfully submit that the method of the present invention recited in Claim 1 is not by the disclosure of Neudeck, et al. since the prior art reference does not disclose each and every element of the claim to which it is applied. Specifically, Neudeck, et al. do not disclose a method in which applicants' claimed step of forming undercutting shallow trench isolation regions is performed such that the back-gate is etched to a length which is less than a length of the overlying Si-containing layer, yet aligned to a lateral edge of said front polySi gate. This step of the claimed method is not disclosed in Neudeck, et al. Instead, Neudeck, et al. provide a method for forming a

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dual-gated SOI FET. The prior art process begins with the formation of a first gate electrode 14 and first oxide layer 15 on an insulating layer 12. Then, a seed hole 17 in the insulating layer 12 is formed exposing the underlying substrate 11. This is followed by the epitaxial lateral overgrowth (ELO) of monocrystalline silicon 18, for example, from the seed hole 17 to on top of the first oxide layer 15. This monocrystalline layer 18 forms the device channel. A second oxide 19 and second gate electrode layer 20 are then grown and deposited, respectively. Subsequent etch steps employing sidewall spacers 23, 25 are then employed to form a multilayered stack having self-aligned first and second gate electrodes, 14 and 20, respectively. Sidewall seed holes are then used to epitaxially grow monocrystalline source and drain regions (30 and 31) from the channel 18. In-situ doping can be provided to form a lightly doped source (LDS) and drain (LDD) structure with vertically displaced source and drain contacts.

Applicants observe that in prior art FIGS. 1F and 1G, oxide sidewalls 27 are formed in an opening formed into the first insulating layer 12. Applicants note that Neudeck, et al. does not disclose the during the forming of this opening that the back-gate 14 is etched to a length which is less than a length of the overlying Si-containing layer 18, yet aligned to a lateral edge of said front polySi gate 20. In the prior art process, etching of back gate 14 is performed, but in the prior art, the etched back gate 14 has a length that extends beyond the length of the overlying Si-containing layer 18. See, for example, FIG. 1F. Applicants further note that the oxide sidewalls 27 disclosed in Neudeck, et al., are formed by oxidation and that the same are different from trench isolation regions.

The foregoing remarks clearly demonstrate that the applied reference does not teach each and every aspect of the method recited in the claims of the present application,

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as required by King and Kloster Speedstell; therefore the claims of the present application are not anticipated by the disclosure of Neudeck, et al. Reconsideration and withdrawal of the rejection under 35 U.S.C. § 102(b) are thus respectfully requested.

In respect to the obviousness rejection to Claim 2 citing the combined disclosures of Neudeck, et al., Komatsu and Stanley Wolf and Richard N. Tuaber, applicants submit that Claim 2 is not rendered obvious over the aforementioned combination of applied references. Specifically, none of the applied references teaches or suggests applicants' claimed method recited in Claim 1 (to which Claim 2 is dependent on) that includes a step in which during the formation of undercutting shallow trench isolation regions, the back-gate is etched to a length which is less than a length of the overlying Si-containing layer, yet aligned to a lateral edge of said front polySi gate.

The principal reference spurring this obviousness rejection, i.e., Neudeck, et al., is defective for the reasons mentioned above in connection with the anticipation rejection. Applicants thus incorporate thus remarks herein by reference. To reiterate: Neudeck, et al. do not teach or suggest that during the formation of shallow trench isolation regions the back-gate is etched to a length which is less than a length of the overlying Si-containing layer, yet aligned to a lateral edge of said front polySi gate. In contrast, Neudeck, et al. disclose a process in which an opening is formed and then sidewall oxide regions 27 are formed. During the formation of the opening, some of the back gate 14 is etched, however, the etching disclosed in the prior art provides a structure in which the back gate 14 has a length that extends beyond the length of the overlying polySi layer 18.

Komatsu does not alleviate the above defects in Neudeck, et al. since the applied reference also does not teach or suggest that during the formation of undercutting shallow trench isolation regions, the back-gate is etched to a length which is less than a length of

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the overlying Si-containing layer, yet aligned to a lateral edge of said front polySi gate. Komtasu provides a semiconductor device including a SOI substrate having a SOI layer, in which a structure made from a semiconductor device is buried. In accordance with the disclosure of Komatsu a thick oxide film is formed on the structure by selectively oxidizing the structure using as a mask an oxidation preventive film formed both on the SOI layer and on a region in which a contact reaching the structure is to be formed; an interlayer dielectric film is then formed on the structure, the SOI layer and the thick oxide film; and a plurality of connection holes are then formed in the interlayer dielectric film and including at least a connection hole positioned on the region in which the contact is to be formed. With this semiconductor device, a contact reaching a back gate electrode can be formed without increasing an aspect ratio of the contact even when a thick oxide film is grown on the back gate electrode in the filed area by selectively oxidizing the back gate electrode in the field area.

Applicants observe that in Komatsu shallow trench isolation regions are not formed, let alone that during the formation of undercutting shallow trench isolation regions, the back-gate is etched to a length which is less than a length of the overlying Si-containing layer, yet aligned to a lateral edge of said front polySi gate. In contrast, Komatsu forms field oxide isolation regions 31 and back gate 15 has a length which extends beyond the length of the overlying SOI layer 10. In view of the above, the combined disclosures of Neudeck, et al. and Komatsu do not render the claimed method obvious.

Stanley Wolf and Richard N. Tauber do not alleviate the above defects in the combined disclosures of Neudeck, et al. and Komatsu since the applied reference also does not teach or suggest a method which includes a process step in which during the

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formation of undercutting shallow trench isolation regions, the back-gate is etched to a length which is less than a length of the overlying Si-containing layer, yet aligned to a lateral edge of said front polySi gate. Indeed, the Stanley Wolf and Richard N. Tauber disclosure is far removed from the claimed invention as evidenced by the Examiner's reliance of the same for disclosing that it is well known to use thermal activation to activate dopants. Applicants do not dispute this, however, Stanley Wolf and Richard N. Tauber do not teach or suggest the claimed feature mentioned above. As such, applicants respectfully submit that the combined disclosures of Neudeck, et al., Komatsu and Stanley Wolf and Richard N. Tauber do not render Claim 2 obvious.

With respect to the obviousness rejection citing the combination of Neudeck, et al. and Stanley Wolf, applicants submit that this combination of references do not render Claims 4 and 17 unpatentable. Specifically, the combination of Neudeck, et al. and Stanley Wolf do not teach or suggest a method in which during the formation of undercutting shallow trench isolation regions, the back-gate is etched to a length which is less than a length of the overlying Si-containing layer, yet aligned to a lateral edge of said front polySi gate. Neudeck, et al. is deficient for the reasons discussed above (See arguments made under the anticipation rejection and the first obviousness rejection).

Stanley Wolf, which discloses that shallow trench isolation regions are known for isolating devices, does not teach or suggest that during the formation of undercutting shallow trench isolation regions, the back-gate is etched to a length which is less than a length of the overlying Si-containing layer, yet aligned to a lateral edge of said front polySi gate. As such, applicants respectfully submit that the combined disclosures of Neudeck, et al., and Stanley Wolf do not render Claims 4 and 17 obvious.

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Insofar as the third obviousness rejection citing the combination of Neudeck, et al. and Komatsu is concerned, applicants respectfully submit that the aforementioned combination does not teach or suggest the claimed method for the reasons discussed in detail in the first obviousness rejection. As such, applicants respectfully submit that the combined disclosures of Neudeck, et al. and Komatsu do not render Claims 6-12 obvious.

The various §103 rejections also fail because there is no motivation in the applied references which suggest modifying the disclosed methods to include applicants' sequence of processing steps recited in Claim 1. Thus, there is no motivation provided in the applied references, or otherwise of record, to make the modification mentioned above. "The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification." In re Vaeck, 947 F.2d, 488, 493, 20 USPQ 2d. 1438, 1442 (Fed.Cir. 1991).

The rejections under 35 U.S.C. §103 have been obviated; therefore reconsideration and withdrawal thereof is respectfully requested.

Thus, in view of the foregoing amendments and remarks, it is firmly believed that the present case is in condition for allowance, which action is earnestly solicited.

Respectfully submitted,

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